AMENDMENTS TO THE CLAIMS

Claim 1 (Currently amended): A method of forming at least one wire on a substrate, the substrate comprising at least one conductive region, an insulating layer disposed on the substrate, and the insulating layer comprising at least one recess exposing the conductive region, the method comprising:

forming a barrier layer on a surface of the insulating layer and the recess;

forming a continuous and uniform conductive layer on a surface of the barrier layer, the conductive layer comprising an aluminum layer or a tungsten layer;

forming a seed layer on a surface of the conductive layer and interlaying the conductive layer between the seed layer and the barrier layer; and

forming a metal layer on a surface of the seed layer, and the metal layer filling up the recess.

Claim 2 (Original): The method of claim 1 wherein the substrate comprises a semiconductor wafer or a silicon-on-insulator substrate (SOI substrate).

Claim 3 (Original): The method of claim 1 wherein the conductive region comprises a source of a transistor, a gate of a transistor, a drain of a transistor, a lower level wire, a landing pad, or a resistor.

Claim 4 (Original): The method of claim 1 wherein the recess is a via hole of a dual damascene structure.

Claim 5 (Original): The method of claim 1 wherein the

barrier layer comprises a silicon nitride layer, a titanium nitride layer (TiN layer), a tantalum nitride layer (TaN layer), or a tantalum nitride/tantalum (TaN/Ta) composite metal layer.

Claim 6 (Canceled)

Claim 7 (Original): The method of claim 1 wherein a thickness of the conductive layer ranges from 5 to 400 angstroms (Å).

Claim 8 (Original): The method of claim 1 wherein the method for forming the conductive layer comprises a chemical vapor deposition (CVD) process or an atomic layer deposition ALD) process.

Claim 9 (Original): The method of claim 1 wherein the seed layer is a copper layer formed by a physical vapor deposition (PVD) process.

Claim 10 (Original): The method of claim 1 wherein the seed layer is a copper alloy layer formed by a physical vapor deposition (PVD) process.

Claim 11 (Original): The method of claim 1 wherein a thickness of the seed layer ranges from 5 to 2000 angstroms (Å).

Claim 12 (Original): The method of claim 1 wherein the metal layer is formed by an electric copper plating (ECP) process.

Claim 13 (Currently amended): A method of forming at least one dual damascene wire on a substrate, the substrate comprising at least one conductive region, an insulating layer disposed on the substrate, and the insulating layer comprising at least one trench pattern and via hole pattern stacked from top to bottom exposing the conductive region, the method comprising:

forming a barrier layer on a surface of the insulating layer, the trench pattern, and the via hole pattern;

forming a continuous and uniform conductive layer on a surface of the barrier layer, the conductive layer comprising an aluminum layer or a tungsten layer;

forming a seed layer on a surface of the conductive layer and interlaying the conductive layer between the seed layer and the barrier layer; and

forming a metal layer on a surface of the seed layer, and the metal layer filling up the trench pattern and the via hole pattern.

Claim 14 (Currently amended): The method of claim 13 wherein the substrate ~~comprise~~ comprises a semiconductor wafer or a silicon-on-insulator substrate (SOI substrate).

Claim 15 (Original): The method of claim 13 wherein the conductive region comprises a source of a transistor, a gate of a transistor, a drain of a transistor, a lower level wire, a landing pad, or a resistor.

Claim 16 (Original): The method of claim 13 wherein the barrier layer comprises a silicon nitride layer, a titanium nitride layer (TiN layer), a tantalum nitride

layer (TaN layer), or a tantalum nitride/tantalum (TaN/Ta) composite metal layer.

Claim 17 (Canceled)

Claim 18 (Original): The method of claim 13 wherein the method for forming the conductive layer comprises a chemical vapor deposition (CVD) process or an atomic layer deposition (ALD) process, and a thickness of the conductive layer ranges from 5 to 400 angstroms (Å).

Claim 19 (Original): The method of claim 13 wherein the seed layer is a copper layer formed by a physical vapor deposition (PVD) process, and a thickness of the seed layer ranges from 5 to 2000 angstroms (Å).

Claim 20 (Original): The method of claim 13 wherein the seed layer is a copper alloy layer formed by a physical vapor deposition (PVD) process, and a thickness of the seed layer ranges from 5 to 2000 angstroms (Å).

Claim 21 (Original): The method of claim 13 wherein the metal layer is formed by an electric copper plating (ECP) process.